LM64C201
Passive Matrix Color LCD Unit

FEATURES

- Display Format: 640 × 480
- Overall Dimensions:
  221.5 (W) × 152.4 (H) × 8.0 (D) mm
- Active Area:
  155.495 (W) × 116.615 (H) mm
- Dot Pitch:
  0.056 × RGB (W) × 0.218 (H) mm

DESCRIPTION

The SHARP LM65C201 is a 640 × 480 dot color display unit consisting of an LCD panel, Printed Wiring Board (PWB) with electric components mounted on it, Tape Automated Bonding (TAB) to connect the LCD panel and PWB electrically, and a plastic chassis with a CCFT backlight and bezel to fit them mechanically. Signal ground (V_{SS}) is connected with the metal bezel.

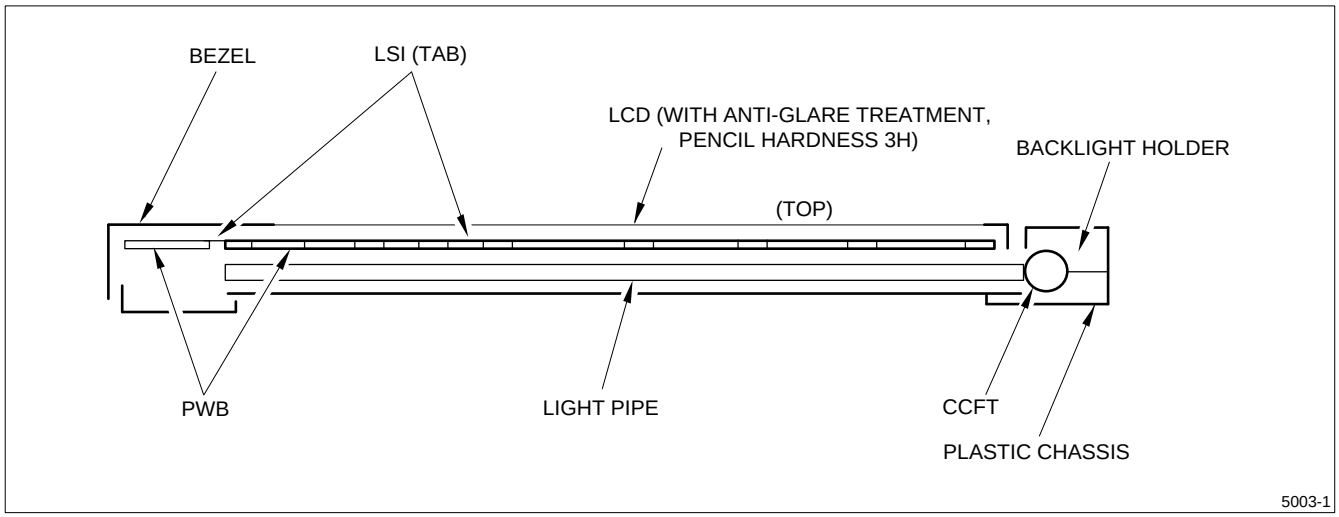


Figure 1. LM64C201 Construction

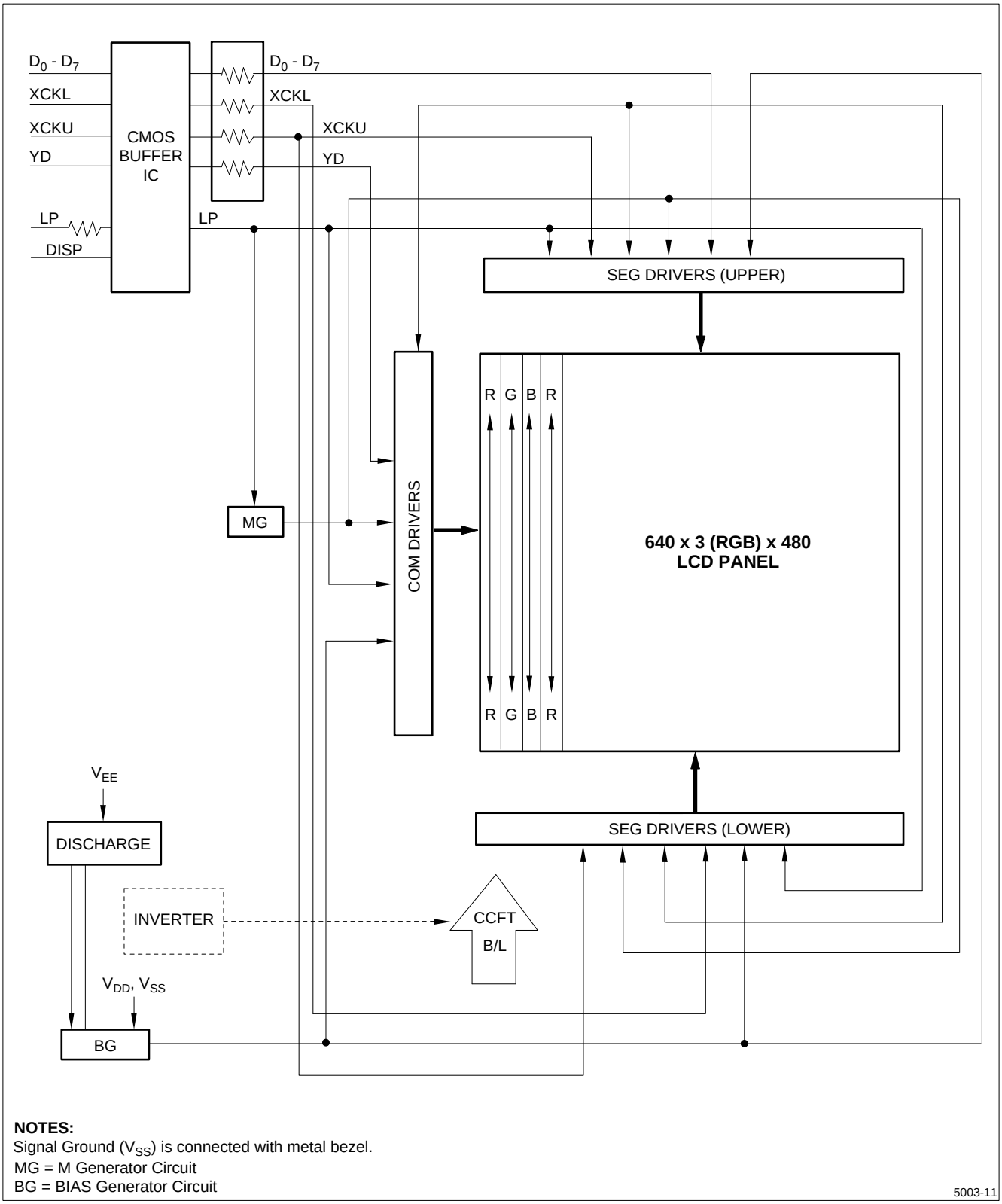


Figure 2. LM64C201 Block Diagram

MECHANICAL SPECIFICATIONS

PARAMETER	SPECIFICATIONS	UNIT	NOTE
Outline Dimensions	221.5 (W) × 152.4 (H) × 8.0 max (D)	mm	1
Active Area	155.495 (W) × 116.615 (H)	mm	
Viewing Area	158.5 (W) × 119.6 (H)	mm	1
Display Format	640 (W) × 480 (H) Full Dots	–	–
Dot Size	0.056 × RGB (W) × 0.218 (H)	mm	–
Dot Spacing	0.025	mm	–
Base Color	Normally Black	–	2, 3
Weight	Approximately 350	g	–

NOTES:

1. Refer to the Outline Dimensions diagram for the tolerance.
2. Due to the characteristics of the LC material, the colors vary with environmental temperature.
3. Negative-type display:
   Display data 'H': Dots ON: Transmission
   Display data 'L': Dots OFF: Light isolation

ABSOLUTE MAXIMUM RATINGS

SYMBOL	PARAMETER	MIN.	MAX.	UNIT	NOTE
$V_{DD} – V_{SS}$	Supply Voltage (Logic)	0	6.0	V	t_A = 25°C
$V_{EE} – V_{SS}$	Supply Voltage (LCD drive)	0	42.0	V	
V_{IN}	Input Voltage	0	V_{DD}	V	

ENVIRONMENTAL CONDITIONS

ITEM	TSTG		TOPR		CONDITION	NOTE
	MIN.	MAX.	MIN.	MAX.		
Ambient Temperature	–25°C	+60°C	0°C	+40°C		1
Humidity					No condensation	2
Vibration					3 Directions (X/Y/Z)	3
Shock					6 Directions (±X ±Y ±Z)	4

NOTES:

1. Do not subject the LCD unit to temperatures out of this specification.
2. $t_A \leq 40°C$, 95% RH maximum.
   $t_A > 40°C$, Absolute humidity less than $t_A = 40°C$ at 95% RH.
3. Two hours for each direction of X/Y/Z (six hours total)

Frequency	10 Hz to 57 Hz	57 Hz to 500 Hz
Vibration Level	–	9.8 m/s^2
Vibration Width	0.075 mm	–
Interval	10 Hz to 500 Hz to 10 Hz/11.0 min	

4. Acceleration: 490 m/s^2
   Pulse width: 11 ms
   Three times for each direction of ±X ±Y ±Z.

ELECTRICAL CHARACTERISTICS (t_A = 25°C, V_{DD} = 5 V ±5%)

SYMBOL	PARAMETER	CONDITION	MIN.	TYP.	MAX.	UNIT	NOTE
$V_{DD} - V_{SS}$	Supply Voltage (Logic)	–	4.75	5.0	5.25	V	–
$V_{EE} - V_{SS}$	Supply Voltage (LCD Drive)	–	30.0	34.4	40.0	V	1, 2
V_{IN}	Input Signal Voltage	'H' Level	0.8 V_{DD}	–	V_{DD}	V	–
		'L' Level	0	–	0.2 V_{DD}	V	–
I_{IL}	Input Leakage Current	'H' Level	–	–	1.0	µA	–
		'L' Level	–1.0	–	–	µA	–
I_{DD}	Supply Current (Logic)	–	–	23.1	34.7	mA	3, 4
I_{EE}	Supply Current (LCD Drive)	–	–	18.7	28.1	mA	3, 4
P_D	Power Consumption	–	–	759	1140	mW	3, 4

NOTES:

1. The viewing angle θ at which the optimum contrast is obtained by adjusting $V_{EE} - V_{SS}$. Refer to Figure 7 for the definition of θ.
2. Maximum and minimum values are specified as the maximum and minimum voltage within the operating temperature range (0 – 40°C). Typical values are specified as the typical voltage at 25°C.
3. Display High Frequency Pattern:
   V_{DD} = 5.0 V, $V_{EE} - V_{SS}$ = 34.4 V, Frame frequency = 73 Hz
   Pattern Display = 4-bit checker
4. This value is direct current.

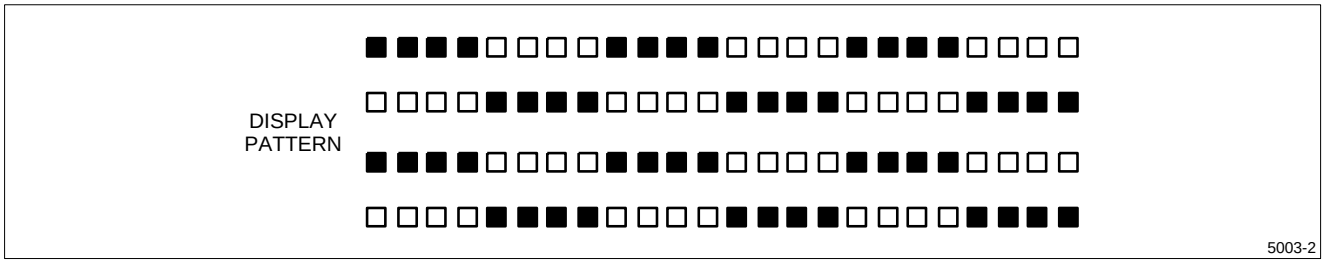


Figure 3. Display High Frequency Pattern

INTERFACE SIGNALS

LCD: CN1 [1]

PIN NUMBER	SYMBOL	PARAMETER	LEVEL
1	YD	Scan Start-up Signal	H
2	LP	Input Data Latch Signal	H → L
3	V_{SS}	Ground Potential	–
4	XCKL	Data Input Clock Signal (Lower)	H → L
5	V_{SS}	Ground Potential	–
6	XCKU	Data Input Clock Signal (Upper)	H → L
7	V_{SS}	Ground Potential	–
8	DISP	Display Control Signal	H (ON), L (OFF)
9	V_{DD}	Power Supply For Logic and LCD	–
10	V_{SS}	Ground Potential	–
11	V_{EE}	Power Supply for LCD (+)	–

LCD: CN2

PIN NUMBER	SYMBOL	PARAMETER	LEVEL
12	V_{SS}	Ground Potential	–
13	D_7	Display Data Signal	H (ON), L (OFF)
14	D_6		
15	D_5		
16	D_4		
17	D_3		
18	D_2		
19	D_1		
20	D_0		
21	V_{SS}	Ground Potential	–

NOTE:

1. Connector used: DF13A-11P-1.25H, DF13A-10P-1.25H (HIROSE)
   Mating connector: DF13-11S-1.25C, DF13-10S-1.25C (HIROSE)

CCFT [1]

PIN NUMBER	SYMBOL	PARAMETER	LEVEL
1	GND	Ground Line (From Inverter)	–
2	NC		–
3	HV	High Voltage Line (From Inverter)	–

NOTE:

1. Connector used: BHR-03VS-1 (JST)
   Mating connector: SM03 (4.0) B-BHS (JST), SM02 (8.0) B-BHS (JST)
   Except above connector shall be out of guaranty.

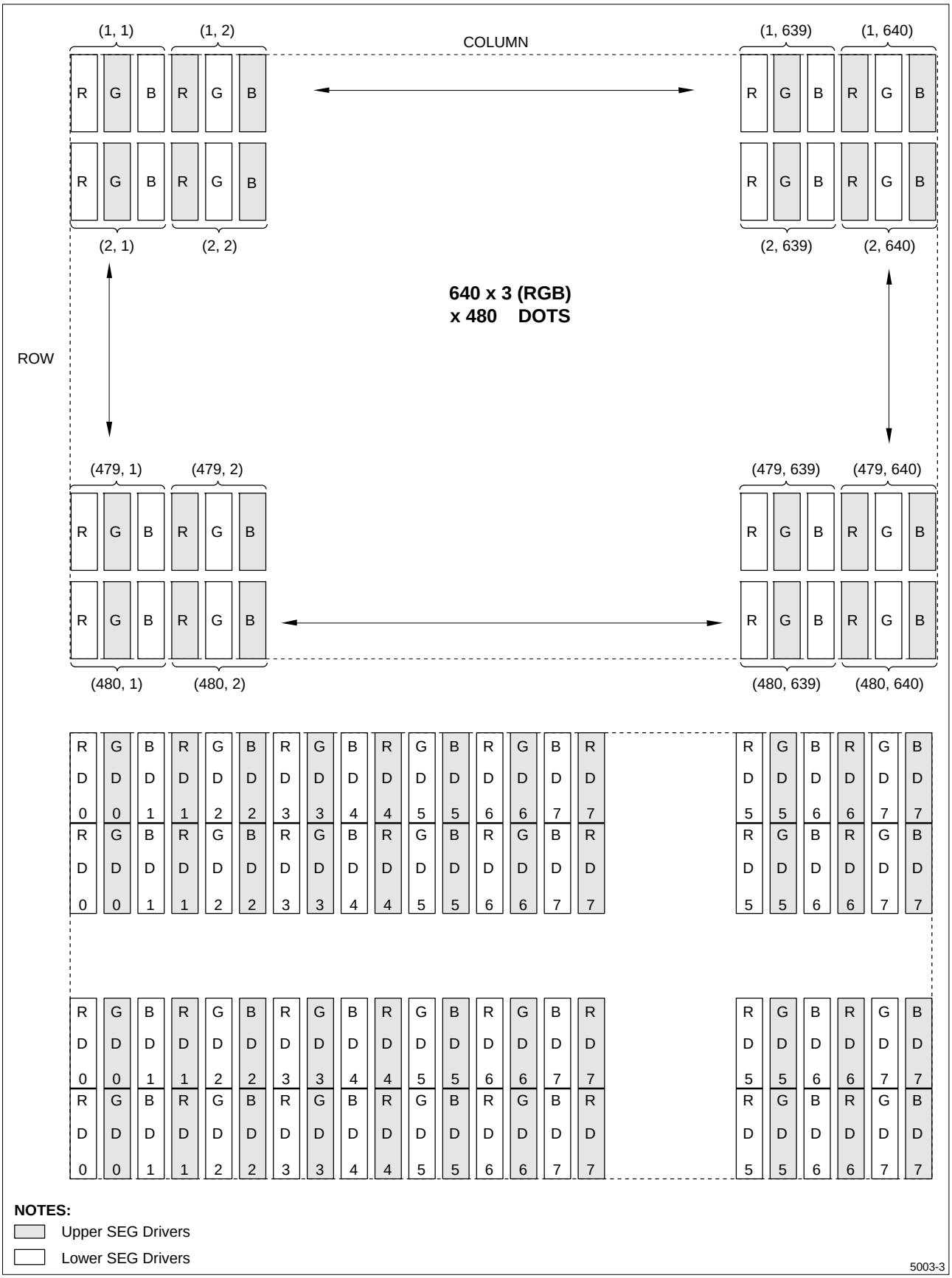


Figure 4. Dot Chart of Display Area

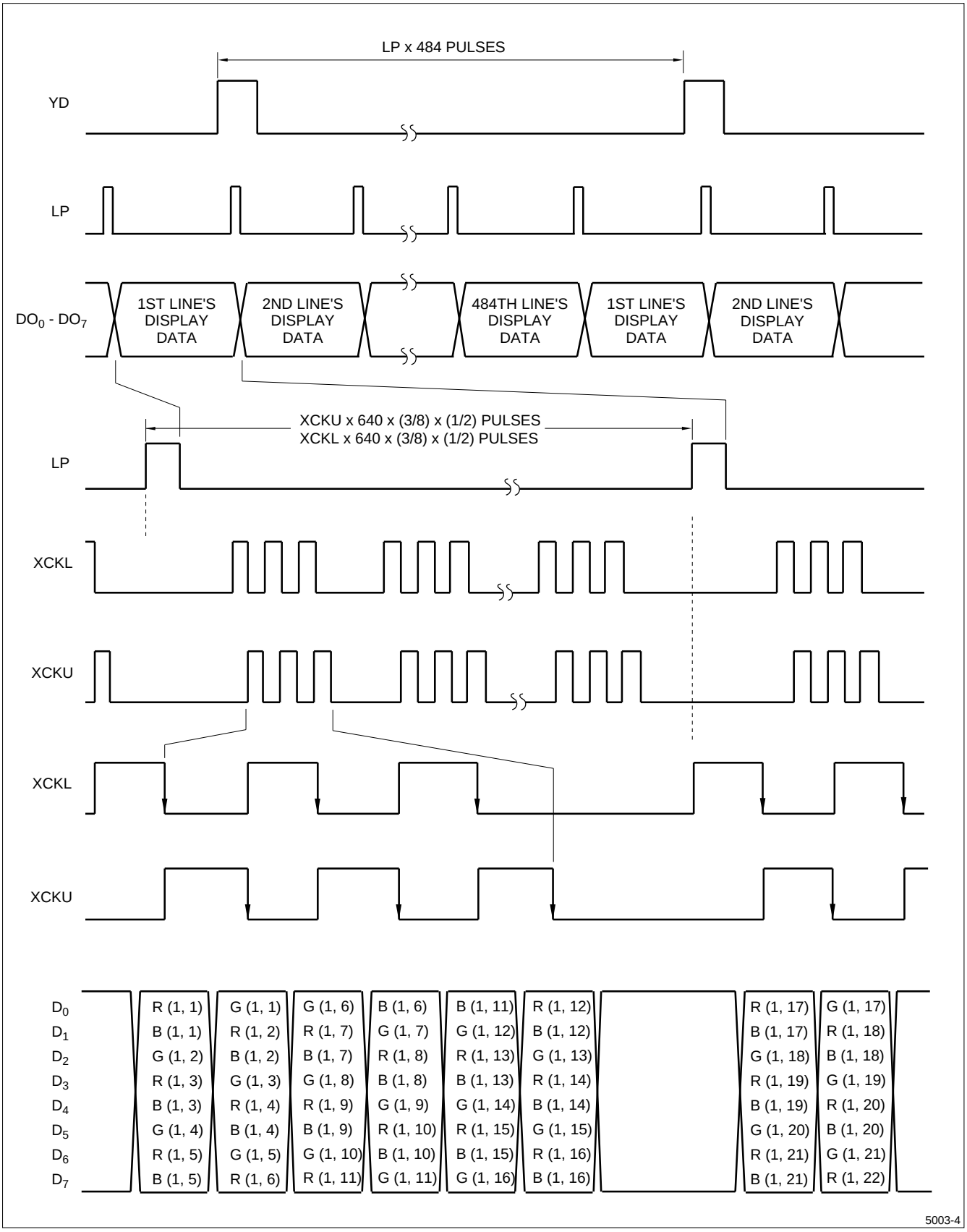


Figure 5. Data Input Timing

INTERFACE TIMING RATINGS

SYMBOL	PARAMETER	MIN.	TYP.	MAX.	UNITS	NOTE
t_{FRM}	Frame Cycle	10.52	–	16.94	ms	1
t_{CK}	XCK Signal Clock Cycled Time	153	–	–	ns	–
t_{WCKH}	XCK Signal 'H' Level Clock Width	50	–	–	ns	–
t_{WCKL}	XCK Signal 'L' Level Clock Width	50	–	–	ns	–
t_{WLPH}	LP Signal 'H' Level Pulse Width	70	–	–	ns	–
t_{DS}	Data Set Up Time	60	–	–	ns	–
t_{DH}	Data Hold Time	60	–	–	ns	–
t_{HYS}	YD Signal 'H' Level Set Up Time	100	–	–	ns	–
t_{HYH}	YD Signal 'H' Level Hold Time	110	–	–	ns	–
t_{LS}	LP ↑ Allowance Time From XCK ↓	200	–	–	ns	–
t_{LH}	XCK ↑ Allowance Time From LP ↓	230	–	–	ns	–
t_R, t_F	Input Signal Rise/Fall Time	–	–	13	ns	–

NOTE:

1. The LCD unit functions at the minimum frame cycle of 10.52 ms (maximum frame frequency of 95 Hz). Due to the characteristics of the LCD unit, 'shadowing' becomes more evident as frame frequency goes up, while flicker is reduced.

   According to our experiments, a minimum frame cycle of 12.8 ms or a maximum frame frequency of 78 Hz demonstrates optimum display quality in terms of flicker and 'shadowing.' Since visual judgment of display quality is subjective, and display quality such as 'shadowing' is pattern dependent, base frame cycle or frame frequency, to which power consumption of the LCD unit is proportional, on thorough testing of the LCD unit with every possible pattern displayed.

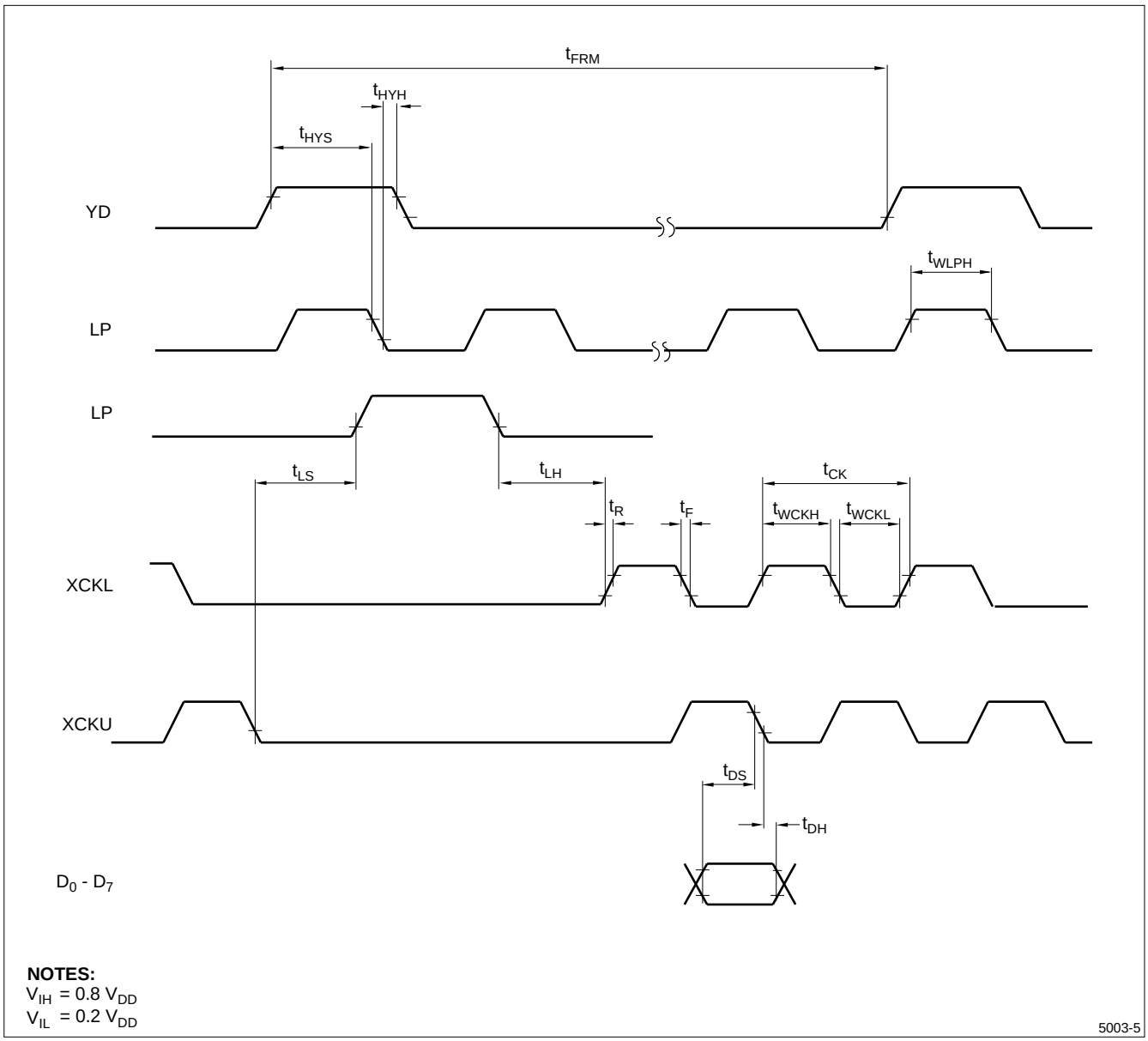


Figure 6. Interface Timing Chart

UNIT DRIVING METHOD

Circuit Driving Method

Figure 2 shows the block diagram of the unit's circuitry.

Display Face Configuration

The display consists of 640 × 3 (RGB) × 480 dots. There is a single panel with single drive driven at 1/484 duty ratio.

Input Data and Control Signal

The LCD driver is 160 bits LSI, consisting of shift registers, latch circuits, and LCD driver circuits. Input data for each row (640 × 3 RGB) is sequentially transferred in the form of 8-bit parallel data through shift registers from the top left of the display face together with the Clock Signal (XCKU, XCKL).

When input of one row (640 × 3 RGB dots) is completed, the data is latched in the form of parallel data corresponding to the signal electrodes by the falling edge of the Latch Signal (LP). Then the corresponding drive signals are transmitted to the 640 × 3 lines of column electrodes of the LCD panel by the LCD drive circuits.

At this time, scan start-up signal (YD) is transferred from the scan signal driver to the first row of scan electrodes, and the contents of the data signals are displayed on the first rows of the display face according to the combinations of voltages applied to the scan and signal electrodes of the LCD. While the first rows of data for 640 × 3 dots are displayed, the second rows of data are entered. When 640 × 3 dots of data have been transferred, they are latched on the falling edge of LP, switching the display to the second row.

Such data input is repeated up to the 484th row of each display segment, from upper to lower rows, to complete one frame of display using the time-sharing method.

The same scanning sequence occurs simultaneously at the lower panel. Then the input proceeds to the next display frame.

YD generates scan signal to drive horizontal electrodes.

Since DC voltage, if applied to LCD panel, causes chemical reaction which deteriorates the LCD panel, drive waveform is inverted at every display frame by Control Signal M to prevent the generation of such DC voltage.

Because of the characteristics of the CMOS driver LSI, the power consumption of the unit goes up with the clock frequency XCKU and XCKL. To minimize data transfer speed of XCKU and XCKL clock, the driver LSI has a system of transferring 8-bits parallel data through the eight lines of shift registers. This system minimizes power consumption of the display unit.

In this circuit configuration, 8-bit display data are input pins $D_0 - D_7$.

The LCD unit also adopts a bus line system for data input to minimize the power consumption. In this system, the data input terminal of each driver LSI activates only when relevant data input is fed.

Data input for column electrodes of both upper and lower display segment and chip select of driver LSI are made as follows:

- The driver LSI at the left end of the display face is first selected, and the adjacent driver LSI of the right side is selected when 160 dots data (20 XCK) is fed. This process continues sequentially until data is fed to the driver LSI at the right end of the display face.
- This process is immediately followed at the column driver's LSIs of both the upper and the lower display segments. Thus, data input for both the upper and the lower display segments must be fed through 8-bit bus line sequentially from the left end of the display face.

Since this graphic display unit contains no refresh RAM, it requires data and timing pulse inputs even for static display.

The timing chart of input signals is shown in Figure 6 and the Interface Timing Ratings table.

OPTICAL CHARACTERISTICS (t_A = 25°C, V_{DD} = 5.0 V, V_{EE} – V_{SS} = V_{MAX})

The following specifications are based on the electrical measuring conditions, on which the contrast of perpendicular direction (θx = θy = 0°) is maximum.

SYMBOL	PARAMETER		CONDITION		MIN.	TYP.	MAX.	UNIT	NOTE
θx	Viewing Angle Range		C_0 > 5.0	θy = 0°	–25	–	25	degrees	1
θy				θx = 0°	–15	–	20		
C_0	Contrast Ratio		θx = θy = 0°		5	13	–	–	2
t_R	Response Time	Rise	θx = θy = 0°		–	280	330	ms	3
t_D	Response Time	Decay	θx = θy = 0°		–	150	200	ms	
x	Unit Chromaticity	White	θx = θy = 0°		–	0.276	–	–	–
y			θx = θy = 0°		–	0.330	–	–	–

NOTES:

1. The viewing angle is defined below.
2. Contrast Ratio is defined as follows:

$$Co = \frac{\text{Luminance (brightness) all pixels 'white' at } V_{MAX}}{\text{Luminance (brightness) all pixels 'dark' at } V_{MAX}}$$

   V_{MAX} is defined in Figure 9.
3. The response characteristics of the photodetector output are measured as shown in Figure 10, assuming that input signals are applied to select and deselect the dots to be measured, in the optical characteristics test method shown in Figure 11.

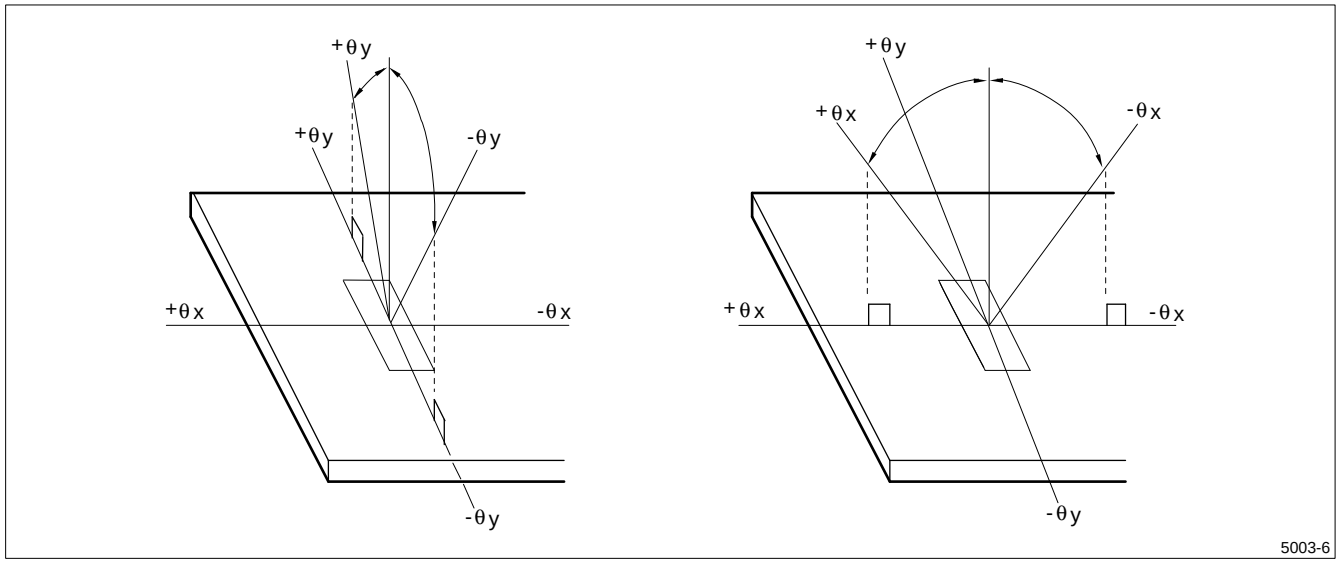


Figure 7. Definition of Viewing Angle

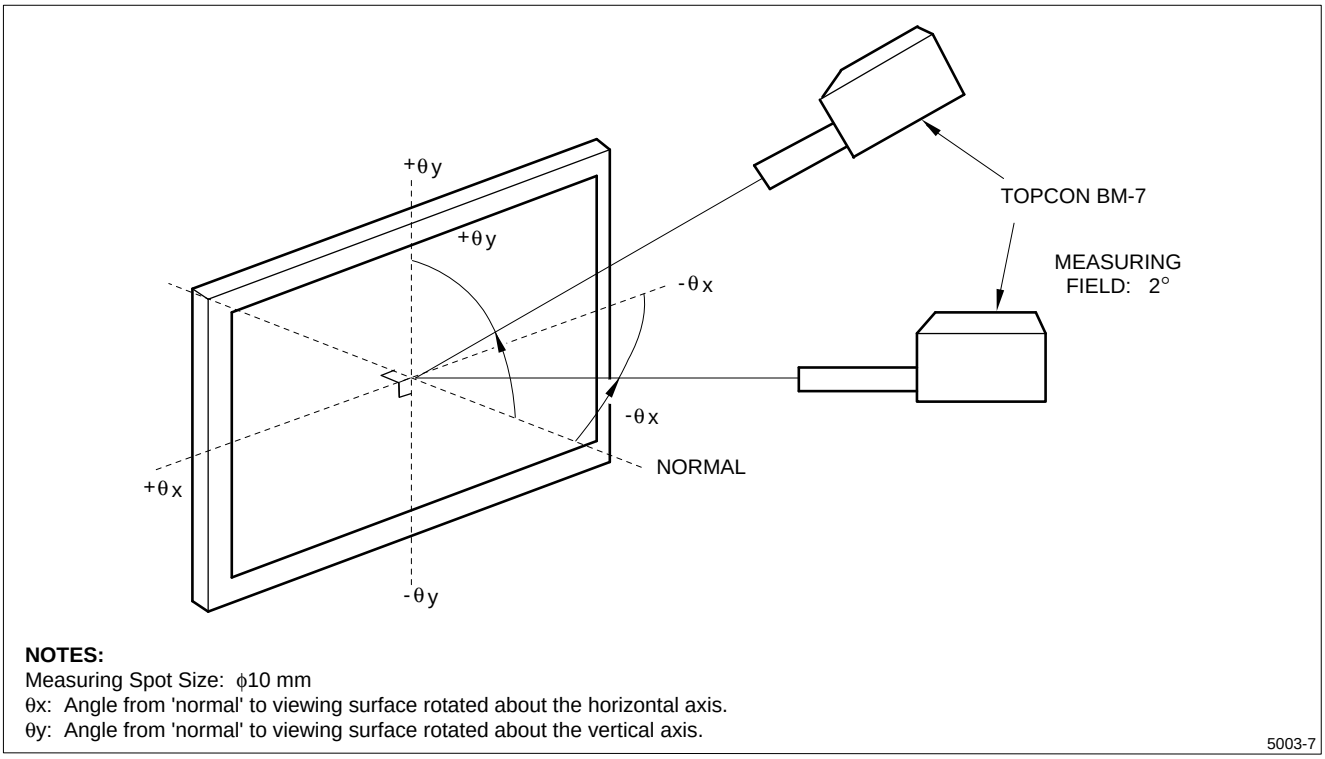


Figure 8. Optical Characteristics Test Method II

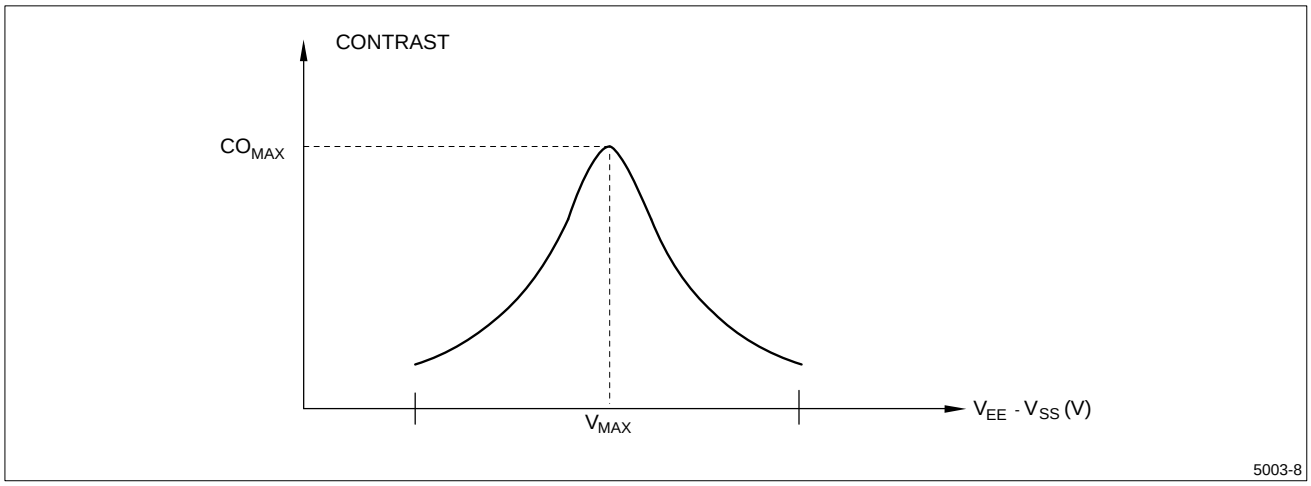


Figure 9. Definition of V_{MAX}

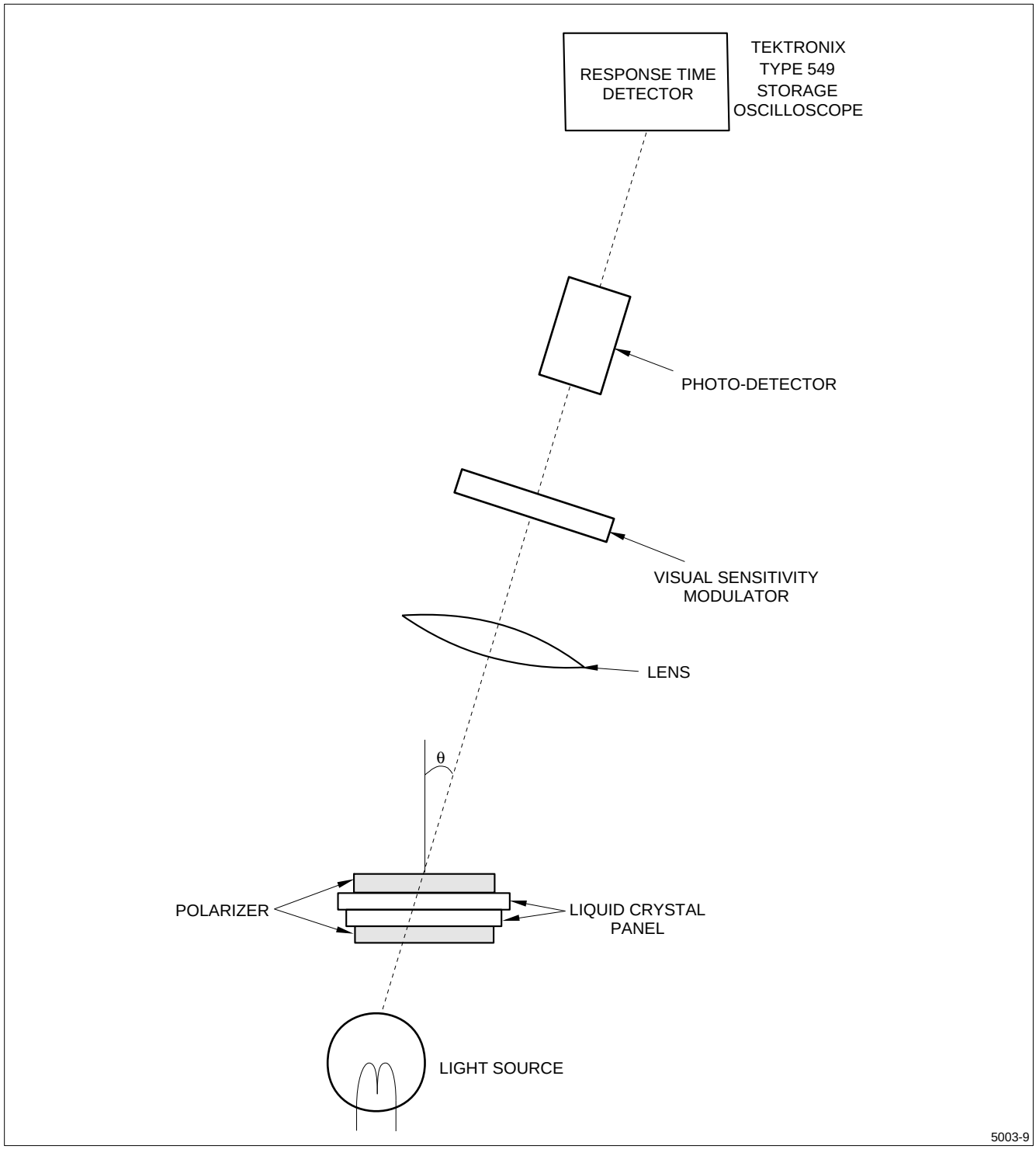


Figure 10. Optical Characteristics Test Method II

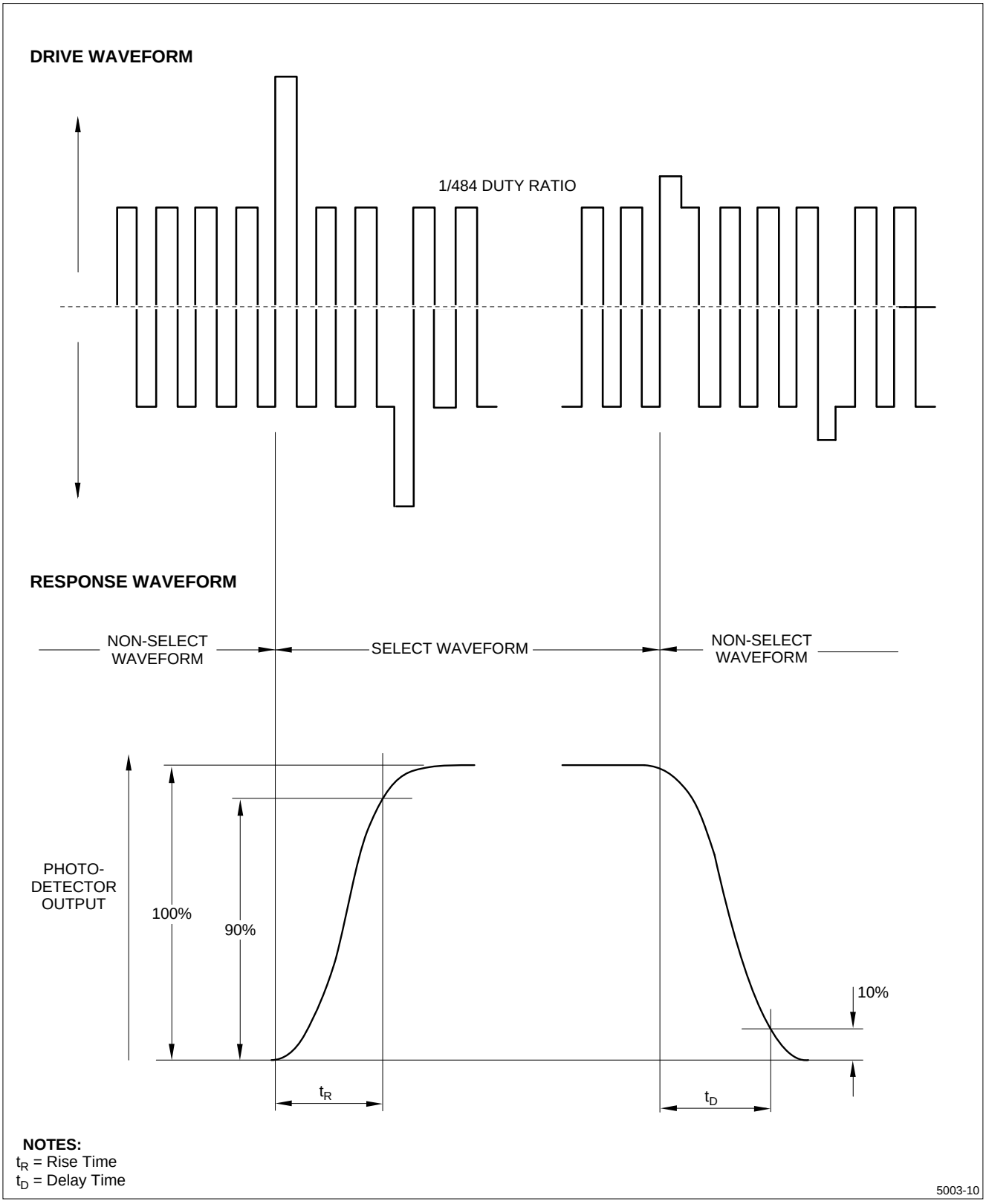


Figure 11. Definition of Response Time

CHARACTERISTICS OF BACKLIGHT

The ratings satisfy the following conditions:

Rating

PARAMETER	MIN.	TY.	MAX.	UNIT
Brightness	40	50	–	cd/m^2

Measurement Circuit

CXA-M10L (TDK) (at IL = 6 mA_{RMS})

Measurement Equipment

BM-7 (TOPCON Corporation)

Measurement Conditions

- Measurement circuit voltage: DC = T.B.D., at primary side.
- LCD: All digits WHITE, V_{DD} = 5 V, $V_{EE} – V_{SS} = V_{MAX}$, $DU_0 – DU_7$ = 'H' (WHITE), $DL_0 – DL_7$ = 'H' (WHITE)
- Ambient temperature: 25°C. Make measurement 30 minutes after turning on the unit.

Lamp Used (Ratings, 1 pc.) [1]

(ELEVAM CORPORATION FLE-26141 (ME) B-NS187)

PARAMETER		MAXIMUM ALLOWABLE VALUE	NOTE
Circuit Voltage (VS)	850 V_{RMS} (minimum)	–	4
Discharging Tube Current (IL)	–	6 mA_{RMS}	2
Power Consumption (P)	2.1 W	–	3
Discharging Tube Voltage (VL)	350 ±32 V_{RMS}	–	–
Brightness (B)	40,000 cd/m^2 (typical)	–	–

NOTES:

1. Within no conductor closed (CCFT only).
2. It is recommended that IL be not more than 6 mA_{RMS} so that heat radiation of CCFT backlight least affects the display quality.
3. Power consumption excluded inverter loss.
4. The circuit voltage (VS) of the inverter should be designed to have some margin (reference value: 1,100 V_{RMS} minimum), because VS may be increased due to leak current in the LCD unit.

Operating Life

The operating lifetime is 10,000 hours or more at 6 mA (operating life with CXA-M10L or equivalent).

The inverter should meet the following conditions:

- Sine, symmetric wave form without spike in positive and negative.
- Output frequency is from 25 kHz to 45 kHz.

Allow for sufficient burn-in time before executing the operating conditions.

The operating lifetime is defined as having ended when any of the following conditions occur (25 ±1°C):

- When the voltage required for initial discharge has reached 1,100 V_{RMS} or when it has reached 10.8 VDC when using an inverter.
- When the illuminence or quantity of light has decreased to 50% of the initial value.

NOTE: Ratings are defined as the average brightness inside the viewing area specified in Figure 12.

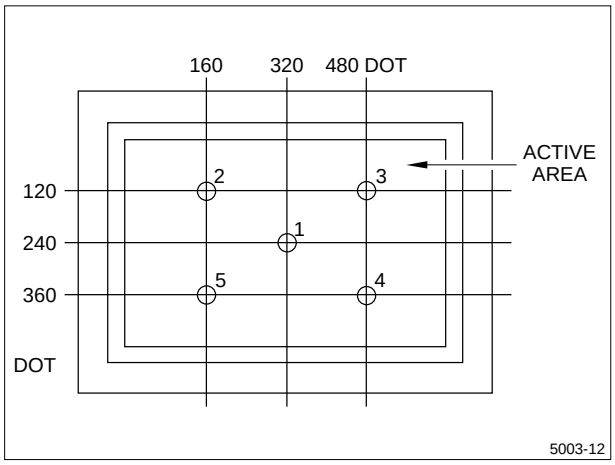


Figure 12. Measuring Points (1 - 5)

PRECAUTIONS

- Industrial (Mechanical) design of the product in which this LCD unit is incorporated must be made so that the viewing angle characteristics of the LCD are optimized. This unit's viewing angle is illustrated in Figure 13 and as follows:
  - θy MIN < viewing angle < θy MAX
    (For the specific values of θy MIN and θy MAX, refer to the Optical Characteristics table.) Consider the optimum viewing conditions according to the purpose when installing the unit.

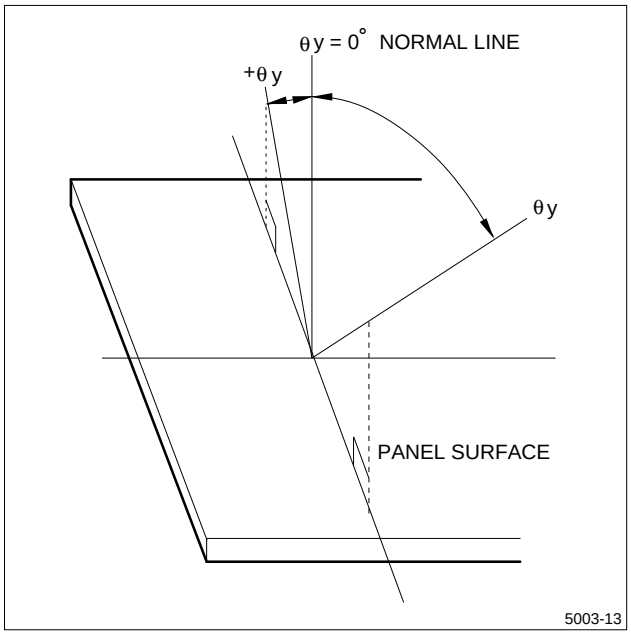


Figure 13. Dot Matrix LCD Viewing Angle

- This unit is installed using mounting tabs at the four corners of PCB or bezel. During installation, avoid undue stress on the unit such as twisting or bending. A transparent acrylic resin board or other type of protective panel should be attached to the front of the unit to protect the polarizer, LCD cells, etc.
- Since the front polarizer is easily damaged, use care to not scratch the face.
- If the surface of the LCD cells need cleaning, wipe it with a soft cloth.
- Wipe liquid off immediately since it can cause color changes and staining.
- The LCD is made of glass plates. Use care when handling it to avoid breakage.
- This unit contains CMOS LSIs which are sensitive to electrostatic charges. The following measures should be taken to protect the unit from electrostatic discharge:
  - Ground the metallic case of the main system (contact of the unit and main system).
  - Insulate the unit and main system by attaching insulating washers made of bakelite or nylon.
- The unit should be driven according to the specified ratings to avoid malfunction or permanent damage. DC voltage drive leads to rapid deterioration of LC, so ensure that the drive is alternating wave form by continuous application of the signal M. Avoid latch-up of driver LSIs and application of DC voltage to the LCD panel by following the ON/OFF sequence shown in Figure 14 and Table 1.
- Since leakage current, which may be caused by routing of CCFT cables, etc., may affect brightness of the display, the inverter has to be designed taking the leakage current into consideration. Thoroughly evaluate the LCD unit/inverter built into the host equipment to ensure the specified brightness.
- Do not expose the unit to direct sunlight, strong ultraviolet light, etc., for prolonged periods.
- Store the unit at normal room temperature to prevent the LC from converting to liquid (due to excessive temperature changes).
- Do not disassemble the unit.

WARNING: Don't use any materials which emit gas from epoxy resin (Amines' hardener) and silicone adhesive agent (dealcohol or deoxym) to prevent polarizer color change caused by gas.

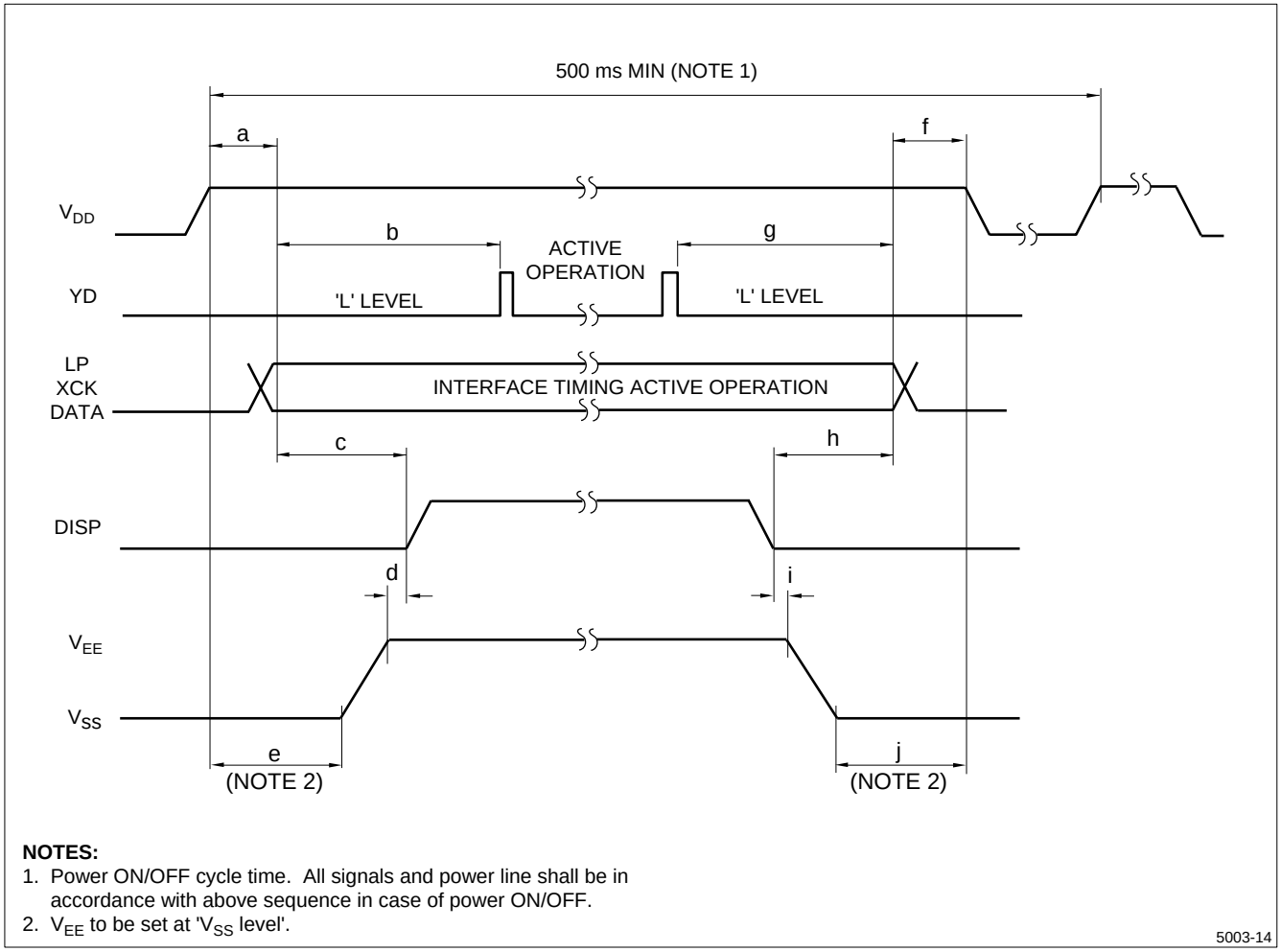


Figure 14. Supply Voltage Sequence Condition

Table 1. Supply Voltage Sequence Condition

SYMBOL	CONDITION
POWER ON	
a	0 ms (minimum)
b	0 ms (minimum)
c	LP × 480 (minimum)
d	0 ms (minimum)
e	0 ms (minimum)
POWER OFF	
f	0 ms (minimum)
g	0 ms (minimum)
h	0 ms (minimum)
i	0 ms (minimum)
j	0 ms (minimum)

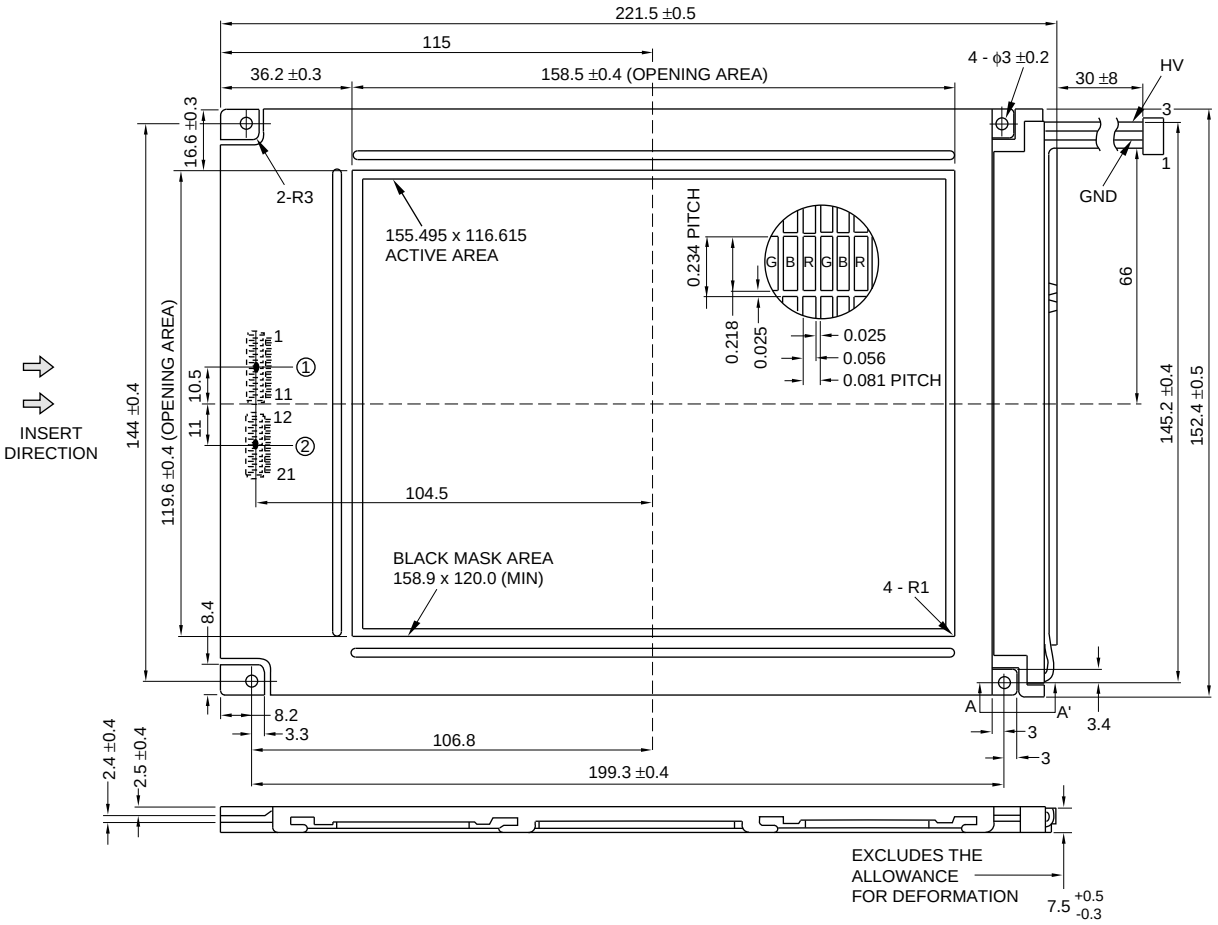
APPLICABLE INSPECTION STANDARD

The LCD unit meets the following inspection standard: S-U-014

DISPLAY QUALITY

This specification describes display quality in case of no gray scale. Since display quality can be affected by gray scale methods, evaluate display quality for the usability of the LCD unit in case gray scale is displayed on the LCD unit.

OUTLINE DIMENSIONS



INTERFACE CONNECTOR PIN LAYOUT

CCFT CONNECTOR PIN LAYOUT
(3 PINS)
BHR-03VS-1 (JST)

PIN #	SYMBOL
1	GND
2	NC
3	HV

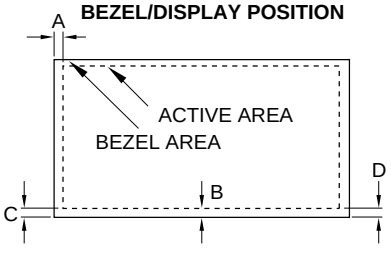
① DF13A-11P-1.25H (HIROSE) (11 PINS)

PIN #	SIGNAL	PIN #	SIGNAL
1	YD	7	V_{SS}
2	LP	8	DISP
3	V_{SS}	9	V_{DD}
4	XCLK	10	V_{SS}
5	V_{SS}	11	V_{EE}
6	XCKU		

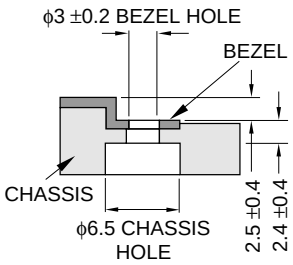
② DF13A-10P-1.25H (HIROSE) (10 PINS)

PIN #	SIGNAL	PIN #	SIGNAL
12	V_{SS}	17	D_3
13	D_7	18	D_2
14	D_6	19	D_1
15	D_5	20	D_0
16	D_4	21	V_{SS}

BEZEL/DISPLAY POSITION



A - A' SECTION



NOTES:
1. Tolerance X-Direction A: 1.5 ±0.8
2. Tolerance Y-Direction B: 1.5 ±0.8
3. Obliquity of Display Area: IC-DI < 0.8

5003-15